What is claimed is:

1. A memory device comprising:

a main memory;

a cache memory connected to the main memory; and

a compression and decompression engine connected between the main memory and the cache memory.

2. The memory device of claim 1 further comprising an error detection and correction engine connected to the main memory and the compression and decompression engine.

3. The memory device of claim 2 wherein the main memory, the cache memory, the compression and decompression engine, and the error detection and correction engine are in the same chip.

4. A memory device comprising:

a main memory;

a cache memory connected to the main memory;

a compression and decompression engine connected between the main memory and the cache memory; and

an error detection and correction engine connected to the main memory and the compression and decompression engine.

5. The memory device of claim 4 wherein the error detection and correction engine is connected between the main memory and the compression and decompression engine.

6. A memory device comprising on a single semiconductor chip:

an input/output buffer;

a cache memory connected to the input/output buffer;

a compression and decompression engine connected to the cache memory; and

a main memory connected to the compression and decompression engine.

7. The memory device of claim 6 wherein the compression and decompression engine is connected between the main memory and the cache memory.

8. The memory device of claim 7 further comprising a error detection and correction engine connected to the main memory and the compression and decompression engine.

9. A system comprising:

a processor; and

a memory device connected to the processor, wherein the memory device comprising a main memory and a compression and decompression engine connected to the main memory.

10. The system of claim 9 wherein the memory device further comprises an error detection correction engine connected to the compression and decompression engine.

11. A system comprising:

a processor;

a cache memory; and

a memory device connected to the processor, wherein the memory device comprises a main memory, a compression and decompression engine connected to the main memory and a cache memory connected to the compression and decompression engine.

12 The system of claim 11 wherein the memory device further comprises an error detection correction engine connected to the compression and decompression engine.

13. The system of claim 11 further comprising a graphic control card, wherein the graphic control card connects to the memory device.

14. The system of claim 11 further comprising a video control card, wherein the video control card connects to the memory device.

15. A method of increasing a storage density of a memory device, comprising:
forming a main memory in a semiconductor chip;
forming a compression and decompression engine in the same chip; and
connecting the compression and decompression engine to the main memory.

16. The method of claim 15 further comprising:
forming a cache memory in the same chip; and
connecting the cache memory to the compression and decompression engine.

17. The method of claim 15 further comprising:
providing an error detection and correction engine; and
connecting the error detection and correction engine to the compression and decompression engine.

18. A method of operating a memory device, comprising:
receiving input data at a cache memory;
compressing the data at a compression and decompression engine to produce compressed data; and
storing the compressed data into a main memory;

19. The method of claim 18 further comprising:
reading the compressed data from the main memory;
decompressing the data at the compression and decompression engine to produced decompressed data; and

reading the decompressed data to the cache memory.

20. A method of operating a memory device, comprising:

forming an input/output buffer;

receiving data at the input/output buffer;

processing the data at a cache memory to produce processed data;

compressing the processed data at a compression and decompression engine to produce compressed data; and

storing the compressed data into a main memory.

21. The method of claim 20 further comprising:

reading data from memory;

decompressing the data at the compression and decompression engine to produced decompressed data;

reading the decompressed data at the cache memory; and

transferring the data to the input/output buffer.